UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,569	12/21/2004	Carl L. Christensen	PU020298	6833

7590 04/27/2010

Joseph S Tripoli
Thomson Licensing Inc
P O Box 5312
Princeton, NJ 08543-5312

EXAMINER	
MALEK, LEILA	
ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
04/27/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/518,569	CHRISTENSEN ET AL.	
	Examiner	Art Unit	
	LEILA MALEK	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-10 and 12-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-10 and 12-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 01/20/2010 have been fully considered but they are not persuasive.

Applicant's Argument: Applicant submits that the combination of Adams and Knapp do not teach or suggest transferring the determined time to a decoding logic circuit for decoding said stream of serialized AES digital audio data by utilizing the determined time, as set forth in claim 1, because Adams merely suggests the transfer of raw clocking data related to the data stream. Nowhere in Adams is the suggestion of transferring the determined time to a decoding logic circuit.

Examiner's Response: Examiner strongly disagrees. Adams does not suggest the transfer of "raw clocking materials", because Adams on page 1, discloses transferring a clock to the decoder (see lines 12-13) and on page 4, lines 26-27 discloses that the clock can be generated based on the amount of time that passes between preamble signals (this clock has been defined by the Applicant as "the determined time"). Therefore the clock transmitted to the decoder as described by Adams is not just a raw clock. Adams clearly teaches transferring the determined time to a decoding logic circuit.

Applicant's Argument: Applicant further argues that in view of Adams, it would not be obvious for one of ordinary skill in the art to first determine a time separating said first and second transitions and then to transfer the determined time to a decoding logic circuit because Adams teaches that the receiver circuits should be capable of tracking

changes in the clocking of the incoming data. In other words, the resources involved in Adams' tracking the changes of the incoming clock data is at the receiving end, not at the transmitting end.

Examiner's Response: Examiner strongly disagrees. Adams on page 4, lines 26-27, states that the generated clock is based on the amount of time that passes between preamble signals. Therefore Adams clearly shows tracking the time that passes between the preamble signals at the transmitter to generate the clock.

Applicant's Argument: Applicant argues that Knapp does not disclose or suggest transferring the determined time to a decoding logic circuit for decoding said stream of serialized AES digital audio data by utilizing the determined time.

Examiner's Response: As explained in the previous office action, Adams discloses transferring the determined time information to a decoding logic circuit (see page 1, lines 12-13 and page 4, lines 26-27). Adams does not disclose decoding the stream of serialized AES digital audio data by utilizing the determined time. However, Knapp discloses a decoder 42 (see column 5, lines 1-28) at the receiver of a communication system, where the decoder continuously decodes the input signal and signals the occurrence of a pattern that matches a predetermined set of valid preambles. Knapp further discloses that the decoder 42 is designed to decode a specific set of bits within the preambles. If that set does not occur for a set period of time, possibly indicated by a certain count within counter 44, then the lock/unlock signal will indicate an unlock condition. Counter 44 is a modulo N counter where N clock cycles is the time period between preambles. If a valid preamble is detected after exactly N clock cycles,

decoder 44 indicates one valid preamble has been detected. Therefore Knapp clearly teaches decoding the data utilizing the determined time between the preambles. It would have been obvious to one of ordinary skill in the art at the time of invention to modify Adams as suggested by Knapp to use the determined time between the preambles to decode the signal, to increase the performance of the decoder by using a more accurate clock.

Applicant's Argument: Applicant further argues that in view of Knapp, it would not be obvious to one of ordinary skill in the art to achieve the claimed invention because Knapp's detection circuit is designed to receive signals, but not for transmitting or transferring the determined time to a decoding logic circuit for decoding said stream of serialized AES digital audio data by utilizing the determined time.

Examiner's Response: Examiner asserts that reference Adams has been used to reject limitations regarding transmitting or transferring the determined time to a decoding logic for decoding said stream of data. Therefore, the combination of Adams and Knapp teaches the limitations argued by the Applicant as explained above.

Applicant's Argument: Applicant argues that neither Scott, nor Adams, separately or in combination, discloses utilizing said extracted time information to decode said received stream of serialized AES digital audio data, as recited in claim 10. Because decoder 708 of Scott separates time division multiplexed data and control information, which is different from the claimed to decode said received stream of serialized AES digital audio data.

Examiner's Response: Examiner asserts that even if for the sake of argument we assume that the decoder 708 only separates the data from the control information, it still decodes the data signal, because it is a decoder. In view of lack of any details on the functionality of the decoder cited in the claim, examiner assumes that the decoder cited in the claim is the same as the Scott's decoder.

Applicant's Argument: Applicant argues that although Lydon discloses that each sub-frame of the AES data stream has 32 bits, Applicants respectfully assert that, in view of Lydon, it would not be obvious to one of ordinary skill in the art to count the number of transitions of the serialized AES digital audio data from the first transition until the number of transition reaches a count of 33, for the simple reason that Lydon teaches away from counting to 33.

Examiner's Response: Examiner asserts that Lydon, in the same field of endeavor, discloses a router, wherein each input of the router is connected to an input processor 14 (see column 1, last paragraph and column 4, lines 29-35). Lydon further discloses that each input processor includes an AES3 receiver 18, which is of conventional form and detects the code violation and locks to the biphase data stream, decodes the biphase mark data to unframed NRZ form, generates output clocks for control purposes and generates overhead bits. Lydon further discloses that the router is a broadcast router (see column 1, third paragraph). Lydon also discloses that the AES sub-frame contains 32 bits (see column 1, lines 25-35) starting with a preamble. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to count the number of transitions of the AES signal from the first transition until the

number of transitions reaches a count of 33 (since it takes 33 counts to reach the preamble in the next sub-frame) to find the second preamble, and also the distance between the preambles, to simplify the detection of the preambles. Since the clock is generated based on the amount of time that passes between preamble signals and according to Lydon it is known that there are exactly 32 bits between the preambles, it would have been obvious to one of ordinary skill in the art at the time of invention to count the number of transitions of the AES signal from the first transition until the number of transitions reaches a count of 33 (since it takes 33 counts to reach the preamble in the next sub-frame) to simply find the second preamble, reduce the complexity of finding the next preamble, and also increase the accuracy of finding it. Furthermore, Examiner asserts that Lydon does not criticize or discredit the counting method, therefore it does not teach away from the claimed subject matter ("the prior art's mere disclosure of more than one alternative does not constitute a teaching away from any of these alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed...." In re Fulton, 391 F.3d 1195, 1201, 73 USPQ2d 1141, 1146 (Fed. Cir. 2004). See also MPEP § 2123).

Claim Objections

2. Claims 1, 10, and 12 are objected to because of the following informalities: as to claims 1, 10, and 12, Applicant needs to define acronym "AES". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adams (W098/16040) (see the IDS) and Knapp et al. (hereafter, referred as Knapp) (US 6,005,904), further in view of Lydon et al. (hereafter, referred as Lydon) (US 6,757,302).

As to claim 1, Adams discloses a method for extracting selected time information from a stream of serialized digital audio data (see page 3, lines 19-31 and page 4, lines 26-27), comprising: detecting a first transition indicative of a first preamble of the stream of serialized AES digital audio data (see page 3, lines 29-31, where Adams describes that each preamble begins with a violation of the biphase-mark encoding rule that each cell is bordered by a transition, and also see page 4, where Adams discloses that the violations have been detected (detection of violations have been interpreted as detection of a first and second preamble, because Adams on page 3, last paragraph discloses that each of the preambles X, Y, and Z, begins with a digital pulse that is 1.5 T in duration- a violation of the biphase-mark encoding rule that each cell is bordered by a transition. Thus each preamble begins with a violation to distinguish the preamble from any other event in the data stream); detecting a second transition indicative of a subsequent preamble of the serialized AES digital audio data; and determining a time

separating the first and second transitions (see page 4, lines 26-27). Adams discloses transferring the determined time information to a decoding logic circuit (see page 1, lines 12-13). Adam discloses all the subject matters claimed in claim 1, except for decoding the data by utilizing the determined time and that the extracting time information (i.e. the steps of detecting and determining) has been performed by a broadcast router. Knapp discloses a decoder 42 (see column 5, lines 1-28) at the receiver of a communication system, where the decoder continuously decodes the input signal and signals the occurrence of a pattern that matches a predetermined set of valid preambles. Knapp further discloses that the decoder 42 is designed to decode a specific set of bits within the preambles. If that set does not occur for a set period of time, possibly indicated by a certain count within counter 44, then the lock/unlock signal will indicate an unlock condition. Counter 44 is a modulo N counter where N clock cycles is the time period between preambles. If a valid preamble is detected after exactly N clock cycles, decoder 44 indicates one valid preamble has been detected. Therefore Knapp clearly teaches decoding the data utilizing the determined time between the preambles. It would have been obvious to one of ordinary skill in the art at the time of invention to modify Adams as suggested by Knapp to use the determined time between the preambles to decode the signal, to increase the performance of the decoder by using a more accurate clock. Adams and Knapp disclose all the subject matters claimed in claim 1, except that that the extracting time information (i.e. the steps of detecting and determining) has been performed by a broadcast router. Lydon, in the same field of endeavor, discloses a router, wherein each input of the router is

connected to an input processor 14 (see column 1, last paragraph and column 4, lines 29-35). Lydon further discloses that each input processor includes an AES3 receiver 18, which is of conventional form and detects the code violation and locks to the biphase data stream, decodes the biphase mark data to unframed NRZ form, generates output clocks for control purposes and generates overhead bits. Lydon further discloses that the router is a broadcast router (see column 1, third paragraph). It would have been obvious to one of ordinary skill in the art at the time of invention to use the teachings of Adams in a broadcast router to take advantage of a self-clocking technique (see Adams pages 2-5).

As to claim 4, Adams, on page 11, lines 26-28, discloses that the time information is determined in the form of a clock pulse count separating the first and second transitions, wherein the clock pulse count is a count of clock pulses. It would have been obvious to one of ordinary skill in the art at the time of invention to modify Adams' background of invention as suggested in Adams' invention disclosure to allow the system to adjust the timing of the clock if necessary (see page 11, lines 28-30).

As to claim 5, Adams does not expressly disclose that the first transition and second transition are separated by thirty one intervening transitions, wherein said thirty one intervening transitions are not indicative of said subsequent preamble of said serialized AES digital audio data. However, it is extremely well known in the art that each sub-frame of AES digital audio data includes 32 bits starting with a preamble, therefore inherently the first transition and second transition are separated by thirty one intervening transitions (i.e. the distance from the preamble in the first sub-frame to the

preamble in the second sub-frame), wherein said thirty one intervening transitions are not indicative of said subsequent preamble of said serialized AES digital audio data.

4. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adams, Knapp, and Lydon, further in view of Lyle et al. (hereafter, referred as Lyle) (US 7,295,578).

As to claim 6, Adams, Knapp and Lydon do not disclose that the determined time information is also suitable for use in encoding the stream. Lyle, in the same field of endeavor, discloses a communication system comprising a transmitter and a receiver (see Fig. 21), wherein a communication link between the transmitter and the receiver feeds back an audio clock signal generated at the receiver (see column 25, lines 56-57) to an encoder of the transmitter (see Fig. 29). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Adams, Knapp, and Lydon as suggested by Lyle to send the clock used for decoding the data to the transmitter to synchronize the clocks used for encoding and decoding.

As to claim 7, Lyle discloses transferring the determined time information to an encoding logic circuit for use in encoding the stream of audio data (see Figs. 21 and 29 and column 25, lines 56-57). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Adams, Knapp, and Lydon as suggested by Lyle to send the clock used for decoding the data to the transmitter to synchronize the clocks used for encoding and decoding.

As to claim 8, Adams, on page 11, lines 26-28, discloses that the time information is determined in the form of a clock pulse count separating the first and

second transitions. It would have been obvious to one of ordinary skill in the art at the time of invention to modify Adam's background of invention as suggested by Adams to allow the system to adjust the timing of the clock if necessary (see page 11, lines 28-30).

As to claim 9, Adams does not expressly disclose that the first transition and second transition are separated by thirty one intervening transitions, wherein said thirty one intervening transitions are not indicative of said subsequent preamble of said serialized AES digital audio data. However, it is extremely well known in the art that each sub-frame of AES digital audio data includes 32 bits (for instance see Lydon lines 25-35) starting with a preamble, therefore inherently the first transition and second transition are separated by thirty one intervening transitions (i.e. the distance from the preamble in the first sub-frame to the preamble in the second sub-frame), wherein said thirty one intervening transitions are not indicative of said subsequent preamble of said serialized AES digital audio data.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Scott et al. (hereafter, referred as Scott) (US 6,654,409), in view of Adams.

As to claim 10, Scott discloses an apparatus comprising: a decoder circuit (see blocks 707 and 708) coupled to receive a stream of serialized (see column 4, lines 27-28) digital audio (i.e. the telephony signal) data (see column 15, lines 24-36), the decoder circuit (combination of blocks 707 and 708) extracting time information from the stream of digital audio data during the decoding thereof; and a target component (see block 712) coupled to the decoder circuit, the target component receiving the extracted

time information from the stream of serialized digital audio data; wherein the target component utilizes the extracted time information while executing at least one function (i.e. encoding) thereof (see column 15, lines 55-56). Scott further discloses that the extracted time information is also utilized, by the decoder circuit, to decode the received stream of serialized digital audio data (see column 15, lines 30-32 time base of the decoder helps the decoder to decode the signal). Scott discloses all the subject matters claimed in claim 10, except that the signal has been encoded according to AES standard. Scott also does not disclose that the time information is based on determining a time separating a first transition, indicative of a first preamble of said stream of serialized AES digital audio data, and a second transition, indicative of a second preamble of said stream of serialized AES digital audio data. However, using AES standard as an encoding standard for digital audio signals is extremely well known in the art (as evidence by Adams page 1, lines 17-27) and therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use AES standard in the system disclosed by Scott to facilitate data transmission between communication devices. Regarding to the second set of limitations missing from Scott, Adams further discloses an apparatus for extracting selected time information from a stream of serialized digital audio data (see page 3, lines 19-31 and page 4, lines 26-27) by detecting a first transition indicative of a first preamble of the stream of serialized AES digital audio data (see page 3, lines 29-31, where Adams describes that each preamble begins with a violation of the biphase-mark encoding rule that each cell is bordered by a transition, and also see page 4, where Adams discloses that the violations have been

detected (detection of violations have been interpreted as detection of a first and second preamble)); detecting a second transition indicative of a subsequent preamble of the serialized AES digital audio data; and determining a time separating the first and second transitions (see page 4, lines 26-27). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Scott as suggested by Adams to take advantage of a self-clocking technique (see Adams page 2, lines 13-19).

6. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fuller (US 6,772,021), in view of Lydon.

As to claim 12, Fuller discloses a method comprising: detecting a first transition of the stream of serialized AES digital audio data (see the abstract, column 1, lines 7-9, 29-34, 48-51, column 2, lines 21-34 and column 3); determining the interval between preambles (see column 2, lines 27-34 and column 3), counting a number of clock pulses of a clock from the detecting of the first transition of the serialized AES digital audio signal in the determined interval (see column 3, first paragraph), and outputting the clock count to a decoding logic circuit (see Fig. 1, blocks 30, 32, and 60, column 2, lines 27-34 and column 3, lines 3-4). Fuller discloses all the subject matters claimed in claim 12, except that that the extracting time information (i.e. the steps of detecting and determining) has been performed by a broadcast router. Fuller also does not disclose that the interval between the preambles has been determined by counting a number of transitions of the serializer AES digital audio data from the first transition until the number of transition reaches a count of 33. As to the first limitation, Lydon, in the same field of endeavor, discloses a router, wherein each input of the router is connected to an

input processor 14 (see column 1, last paragraph and column 4, lines 29-35). Lydon further discloses that each input processor includes an AES3 receiver 18, which is of conventional form and detects the code violation and locks to the biphase data stream, decodes the biphase mark data to unframed NRZ form, generates output clocks for control purposes and generates overhead bits. Lydon further discloses that the router is a broadcast router (see column 1, third paragraph). It would have been obvious to one of ordinary skill in the art at the time of invention to use the teachings of Adams in a broadcast router to take advantage of a self-clocking technique (see Adams pages 2-5). As to the second limitation, Lydon discloses that the AES sub-frame contains 32 bits (see column 1, lines 25-35) starting with a preamble. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to count the number of transitions of the AES signal from the first transition until the number of transitions reaches a count of 33 (since it takes 33 counts to reach the preamble in the next sub-frame) to find the second preamble, and also the distance between the preambles, to simplify the detection of the preambles.

As to claim 13, Fuller discloses that the clock is a higher frequency than a frequency of the transitions of the serialized AES audio data (see column 2, lines 60-62).

As to claim 14, Fuller discloses that the clock is a fast clock (see column 2, lines 60-62, because the clock is preferably at least 4, and more preferably at least 8 or 16, times the rate of the audio data).

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEILA MALEK whose telephone number is (571)272-8731. The examiner can normally be reached on 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Leila Malek
Examiner
Art Unit 2611

/L. M./
/Leila Malek/
Examiner, Art Unit 2611

/Mohammad H Ghayour/
Supervisory Patent Examiner, Art Unit 2611